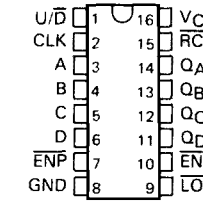
SYNCHRONOUS 4-BIT UP/DOWN DECADE AND BINARY COUNTERS

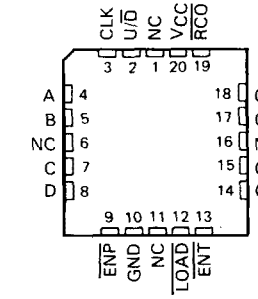
MARCH 1984 – REVISED MAY 1986

- **Fully Synchronous Operation for Counting and Programming**
- **Internal Look-Ahead for Fast Counting**
- **Carry Output for n-Bit Cascading**
- **Fully Independent Clock Circuit**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS', SN54AS' . . . J PACKAGE
SN74ALS', SN74AS' . . . D OR N PACKAGE
(TOP VIEW)



SN54ALS', SN54AS' . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These synchronous presettable counters feature an internal carry look-ahead for cascading in high-speed counting applications. The 'ALS168B and 'AS168 are decade counters and the 'ALS169B and 'AS169 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation helps eliminate the output counting spikes that are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock waveform.

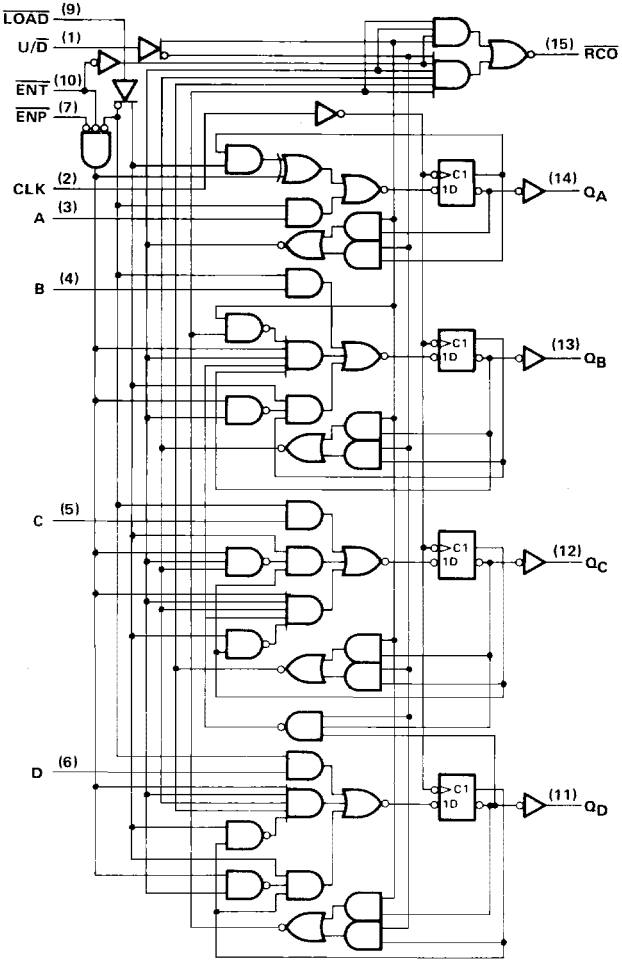
These counters are fully programmable; that is, the outputs may each be preset to either level. The load input circuitry allows loading with the carry-enable output of cascaded counters. As loading is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the data inputs after the next clock pulse.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous application without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a carry output. Both count enable inputs ($\overline{ENP}$ and $\overline{ENT}$) must be low to count. The direction of the count is determined by the level of the U/$\overline{D}$ input. When U/$\overline{D}$ is high, the counter counts up; when low, it counts down. Input $\overline{ENT}$ is fed forward to enable the carry output. The riple carry output ($\overline{RCO}$) thus enabled will produce a low-level pulse while the count is zero (all inputs low) counting down or maximum (9 or 15) counting up. This low-level overflow carry pulse can be used to enable successive cascaded stages. Transistions at $\overline{ENP}$ or $\overline{ENT}$ are allowed regardless of the level of the clock input. All inputs are diode-clamped to minimize transmission-line effects, thereby simplifying system design.

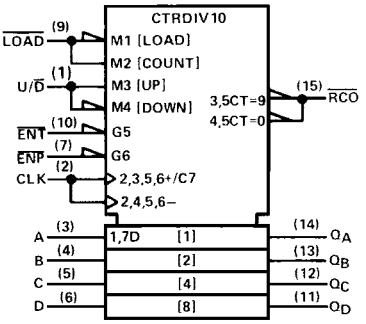
These counters feature a fully independent clock circuit. Changes at control inputs ($\overline{ENP}$, $\overline{ENT}$, $\overline{LOAD}$, U/$\overline{D}$) that will modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

The SN54ALS168B, SN54AS168, SN54ALS169B, and SN54AS169 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS168B, SN74AS168, SN74ALS169B, and SN74AS169 are characterized for operation from 0°C to 70°C.

'ALS168B, 'AS168 logic diagram (positive logic)



'ALS168B, 'AS168 logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

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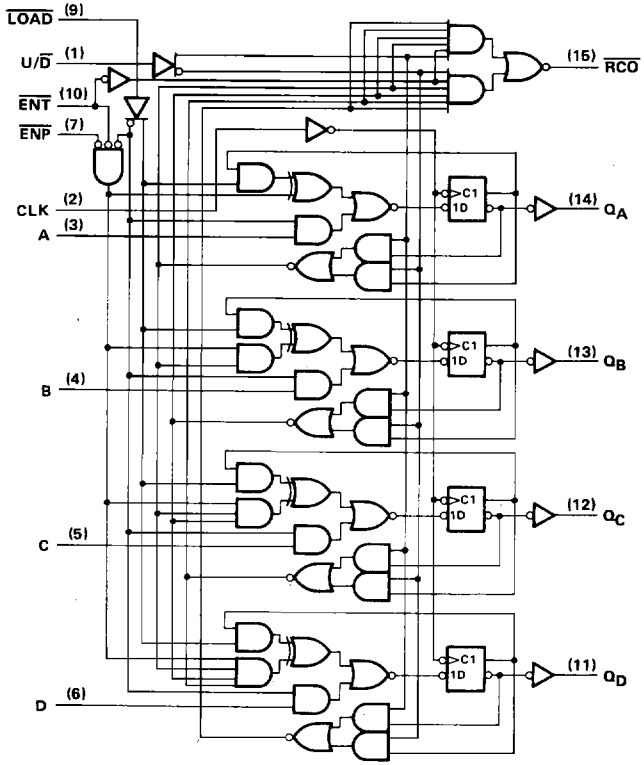
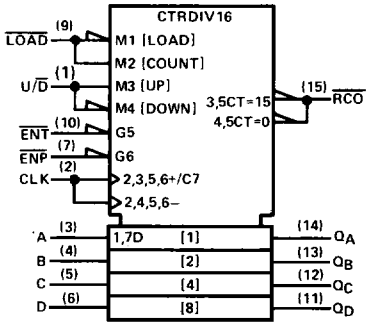
'ALS169B, 'AS169 logic diagram (positive logic)



'ALS169B, 'AS169 logic symbol†

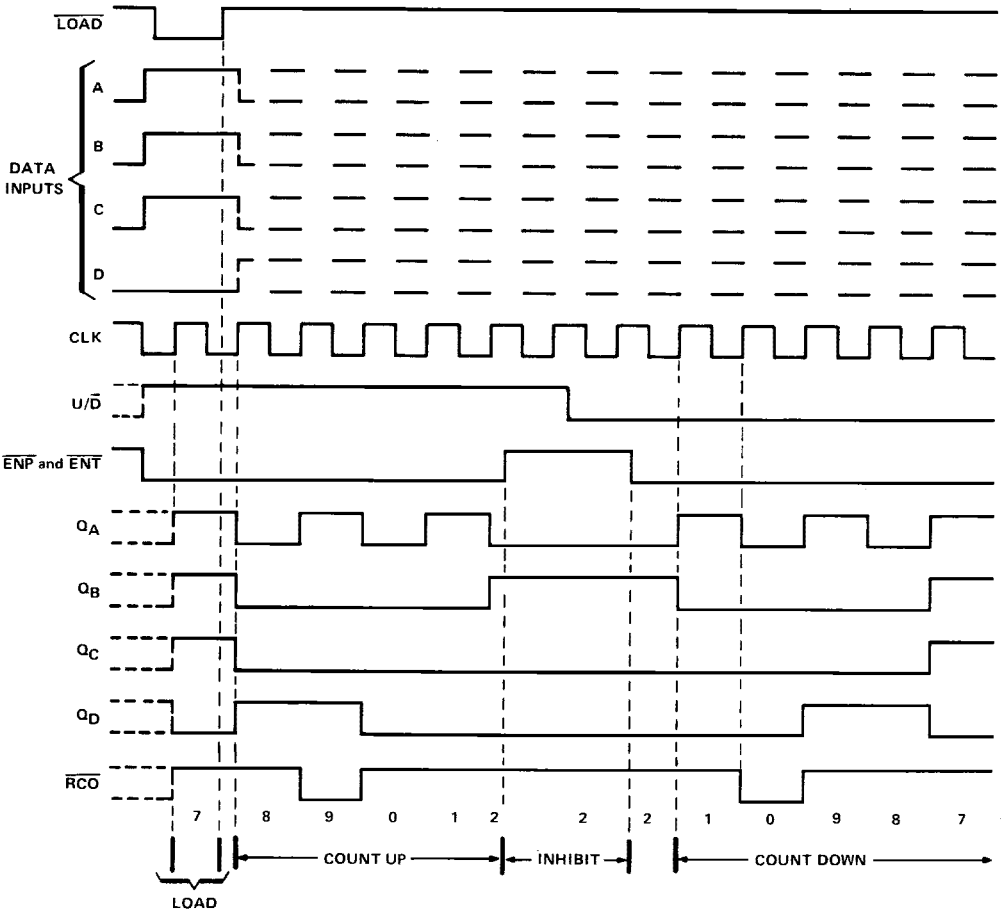


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

'ALS168B, 'AS168 typical load, count, and inhibit sequences

Illustrated below is the following sequence:

1. Load (preset) to BCD seven
2. Count up to eight, nine (maximum), zero, one, and two
3. Inhibit
4. Count down to one, zero (minimum), nine, eight, and seven



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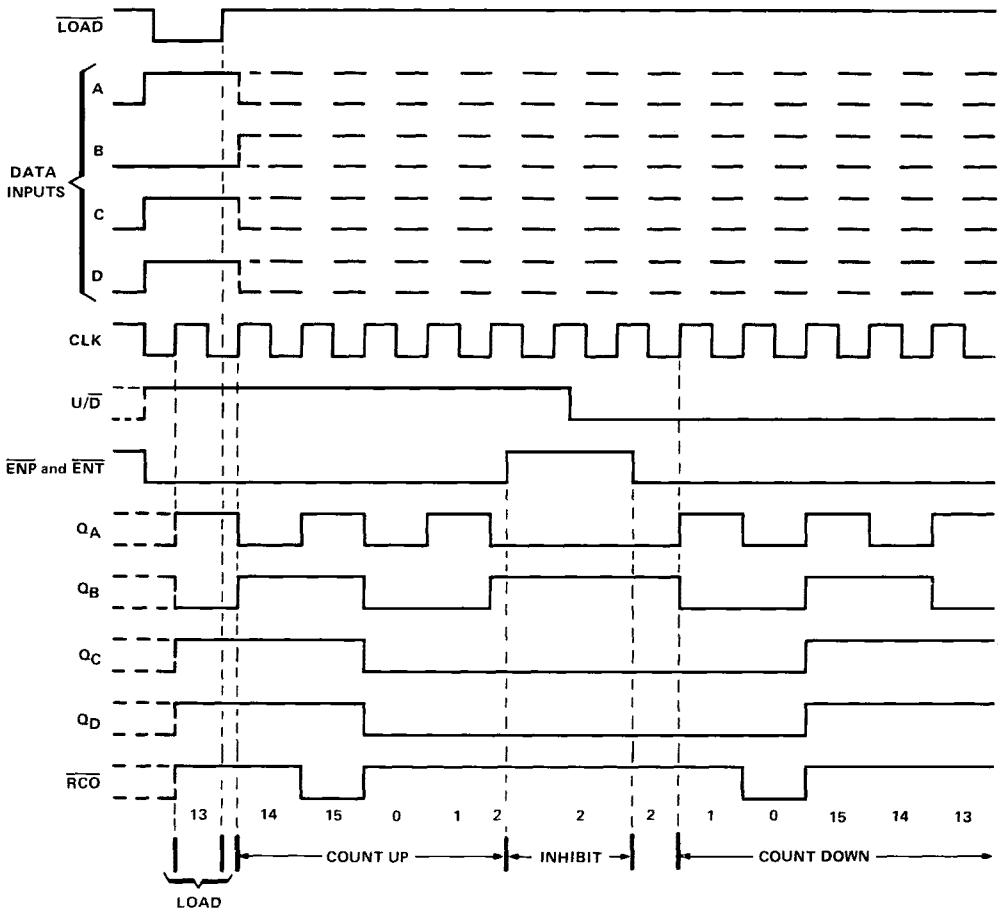
'ALS169B, 'AS169 typical load, count, and inhibit sequences

Illustrated below is the following sequence:

1. Load (preset) to binary thirteen
2. Count up to fourteen, fifteen (maximum), zero, one, and two
3. Inhibit
4. Count down to one, zero (minimum), fifteen, fourteen, and thirteen



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS168B, SN54ALS169B . . . . . −55°C to 125°C
SN74ALS168B, SN74ALS169B . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54ALS168B SN54ALS169B			SN74ALS168B SN74ALS169B			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
I_{OH}	High-level output current				−0.4			−0.4	mA
I_{OL}	Low-level output current				4			8	mA
f_{clock}	Clock frequency		0		22	0		40	MHz
t_w	Pulse duration	CLK high or low	14			12.5			ns
t_{su}	Setup time before CLK↑	A, B, C, or D	20			15			ns
		$\overline{ENP}$ or $\overline{ENT}$	25			15			
		$\overline{LOAD}$	20			15			
		U/$\overline{D}$	28			15			
t_h	Hold time, data after CLK↑		0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS168B SN54ALS169B			SN74ALS168B SN74ALS169B			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V			15	25		15	25	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

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'ALS168B, 'ALS169B switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS168B SN54ALS169B		SN74ALS168B SN74ALS169B		
			MIN	MAX	MIN	MAX	
f_{max}			22		40		MHz
t_{PLH}	CLK	$\overline{RCO}$	3	25	3	20	ns
t_{PHL}			6	25	6	20	
t_{PLH}	CLK	Any Q	2	20	2	15	ns
t_{PHL}			5	23	5	20	
t_{PLH}	$\overline{ENT}$	$\overline{RCO}$	2	16	2	13	ns
t_{PHL}			3	24	3	16	
t_{PLH}	U/$\overline{D}$	$\overline{RCO}$	5	22	5	19	ns
t_{PHL}			5	22	5	19	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS168, SN54AS169 . . . . . −55 °C to 125 °C
SN74AS168, SN74AS169 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

			SN54AS168 SN54AS169			SN74AS168 SN74AS169			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−2			−2	mA
I_{OL}	Low-level output current				20			20	mA
f_{clock}	Clock frequency		0		65	0		75	MHz
t_w	Pulse duration	CLK high or low	7.7			6.7			ns
t_{su}	Setup time before CLK↑	A, B, C, or D	10			8			ns
		$\overline{ENP}$ or $\overline{ENT}$	10			8			
		$\overline{LOAD}$	10			8			
		U/$\overline{D}$	10			8			
t_h	Hold time, data after CLK↑		2			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS168 SN54AS169			SN74AS168 SN74AS169			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.25	0.5		0.25	0.5	V
I_I	$\overline{LOAD}$, $\overline{ENT}$, U/$\overline{D}$	V_{CC} = 5.5 V,	V_I = 7 V			0.2			0.2	mA
	All others					0.1			0.1	
I_{IH}	$\overline{LOAD}$, $\overline{ENT}$, U/$\overline{D}$	V_{CC} = 5.5 V,	V_I = 2.7 V			40			40	μA
	All others					20			20	
I_{IL}	$\overline{LOAD}$, $\overline{ENT}$, U/$\overline{D}$	V_{CC} = 5.5 V,	V_I = 0.4 V			−1			−1	mA
	All others,					−0.5			−0.5	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V			41	63		41	63	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

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'AS168, 'AS169 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS168 SN54AS169		SN74AS168 SN74AS169		
			MIN	MAX	MIN	MAX	
f_{max}			65		75		MHz
t_{PLH}	CLK	$\overline{RCO}$	3	17.5	3	16.5	ns
t_{PHL}		($\overline{LOAD}$ high or low)	2	14	2	13	
t_{PLH}	CLK	Any Q	1	7.5	1	7	ns
t_{PHL}			2	14	2	13	
t_{PLH}	$\overline{ENT}$	$\overline{RCO}$	1.5	10	1.5	9	ns
t_{PHL}			1.5	10	1.5	9	
t_{PLH}	U/$\overline{D}$	$\overline{RCO}$	2	14	2	12	ns
t_{PHL}			2	14.5	2	13	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.