

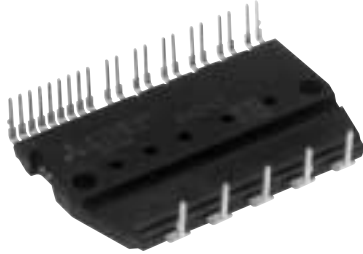
# PS21564-P

TRANSFER-MOLD TYPE  
INSULATED TYPE

## PS21564-P

### INTEGRATED POWER FUNCTIONS

600V/15A low-loss 5<sup>th</sup> generation inverter bridge for three phase DC-to-AC power conversion



### INTEGRATED DRIVE, PROTECTION AND SYSTEM CONTROL FUNCTIONS

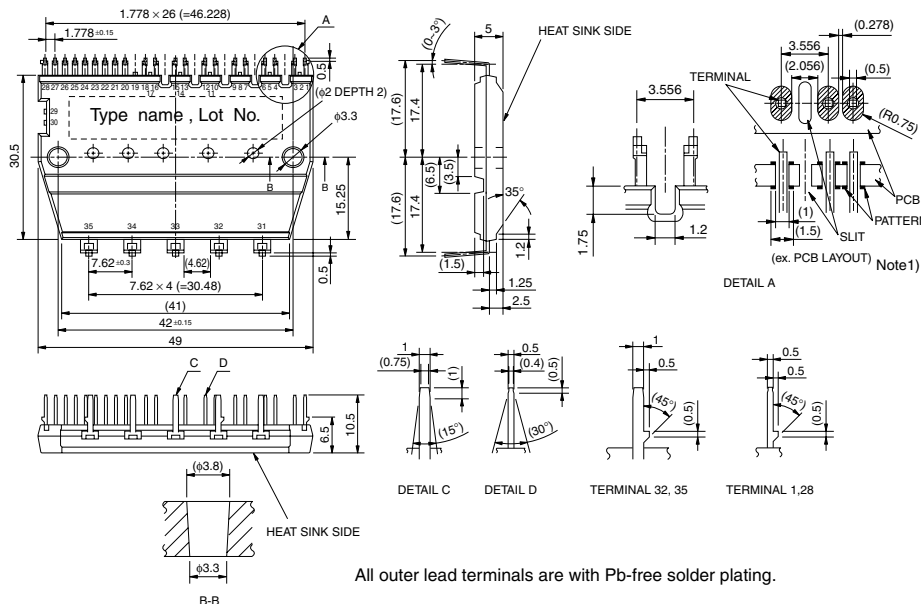
- For upper-leg IGBTs : Drive circuit, High voltage isolated high-speed level shifting, Control supply under-voltage (UV) protection.
- For lower-leg IGBTs : Drive circuit, Control supply under-voltage protection (UV), Short circuit protection (SC).
- Fault signaling : Corresponding to an SC fault (Lower-leg IGBT) or a UV fault (Lower-side supply).
- Input interface : 3, 5V line CMOS/TTL compatible. (High Active)
- UL Approved : Yellow Card No. E80276

## APPLICATION

AC100V~200V inverter drive for small power motor control.

Fig. 1 PACKAGE OUTLINES

Dimensions in mm



All outer lead terminals are with Pb-free solder plating.

- Note 1 :** In order to get enough creepage distance between the terminals, please take some countermeasure such as a slit on PCB.  
**2 :** Treat the terminal Vno of PS21564-P as NC. (just the same as DIP-IPM ver.2) However, external connection of Vno with N terminals is necessary for PS21562-P or PS21563-P.

Fig. 2 INTERNAL FUNCTIONS BLOCK DIAGRAM (TYPICAL APPLICATION EXAMPLE)

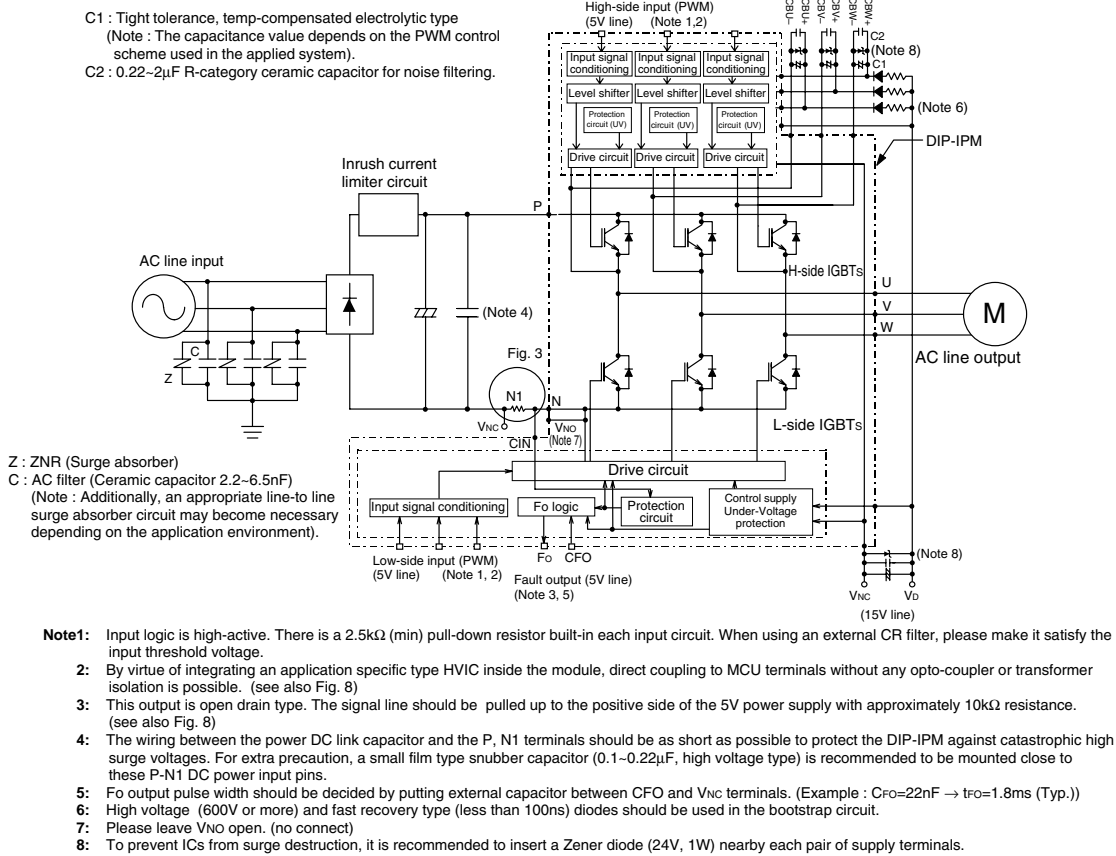
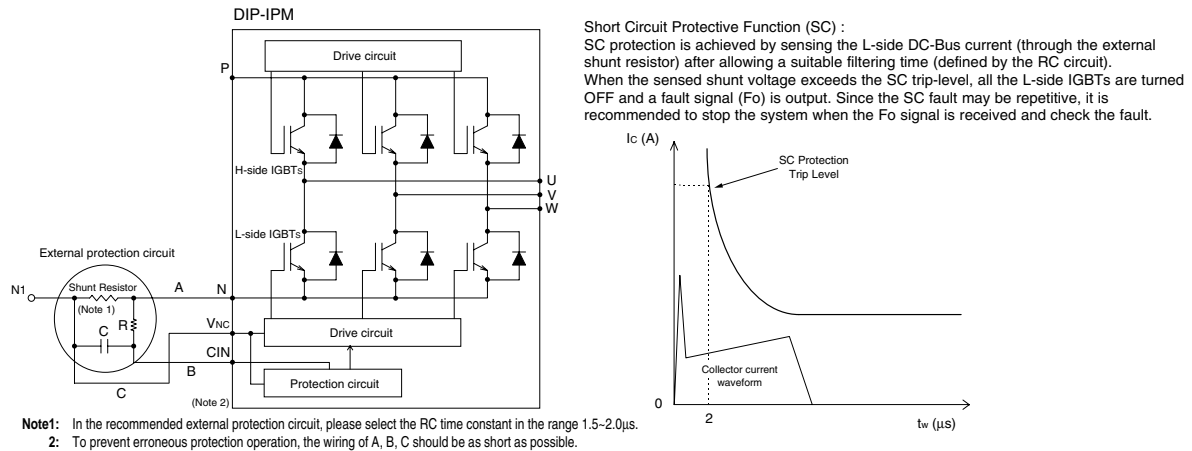


Fig. 3 EXTERNAL PART OF THE DIP-IPM PROTECTION CIRCUIT



**PS21564-P**

TRANSFER-MOLD TYPE  
INSULATED TYPE

**MAXIMUM RATINGS** ( $T_j = 25^\circ\text{C}$ , unless otherwise noted)

**INVERTER PART**

Symbol	Parameter	Condition	Ratings	Unit
VCC	Supply voltage	Applied between P-N	450	V
VCC(surge)	Supply voltage (surge)	Applied between P-N	500	V
VCEs	Collector-emitter voltage		600	V
$\pm I_C$	Each IGBT collector current	$T_f = 25^\circ\text{C}$	15	A
$\pm I_{CP}$	Each IGBT collector current (peak)	$T_f = 25^\circ\text{C}$ , less than 1ms	30	A
PC	Collector dissipation	$T_f = 25^\circ\text{C}$ , per 1 chip	22.2	W
$T_j$	Junction temperature	(Note 1)	-20~+125	$^\circ\text{C}$

**Note 1** : The maximum junction temperature rating of the power chips integrated within the DIP-IPM is  $150^\circ\text{C}$  ( $@ T_f \leq 100^\circ\text{C}$ ) however, to ensure safe operation of the DIP-IPM, the average junction temperature should be limited to  $T_{j(ave)} \leq 125^\circ\text{C}$  ( $@ T_f \leq 100^\circ\text{C}$ ).

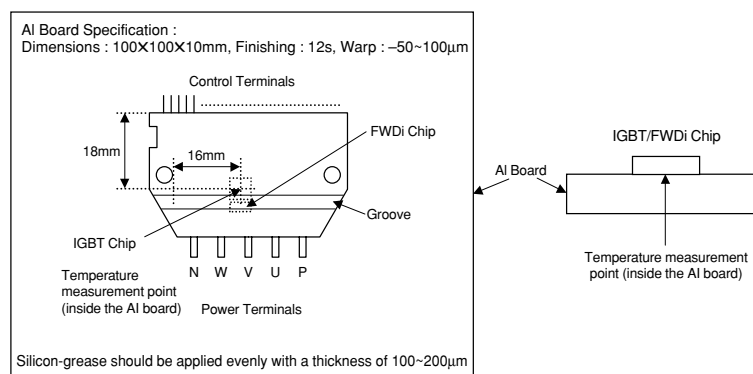
**CONTROL (PROTECTION) PART**

Symbol	Parameter	Condition	Ratings	Unit
V <sub>D</sub>	Control supply voltage	Applied between VP1-VNC, VN1-VNC	20	V
V <sub>DB</sub>	Control supply voltage	Applied between VUFB-VUFS, VVFB-VVFS, VWFB-VWFS	20	V
V <sub>IN</sub>	Input voltage	Applied between UP, VP, WP, UN, VN, WN-VNC	-0.5~V <sub>D</sub> +0.5	V
V <sub>FO</sub>	Fault output supply voltage	Applied between FO-VNC	-0.5~V <sub>D</sub> +0.5	V
I <sub>FO</sub>	Fault output current	Sink current at FO terminal	1	mA
V <sub>SC</sub>	Current sensing input voltage	Applied between CIN-VNC	-0.5~V <sub>D</sub> +0.5	V

**TOTAL SYSTEM**

Symbol	Parameter	Condition	Ratings	Unit
VCC(PROT)	Self protection supply voltage limit (short circuit protection capability)	V <sub>D</sub> = 13.5~16.5V, Inverter part $T_j = 125^\circ\text{C}$ , non-repetitive, less than 2 $\mu\text{s}$	400	V
T <sub>f</sub>	Module case operation temperature	(Note 2)	-20~+100	$^\circ\text{C}$
T <sub>stg</sub>	Storage temperature		-40~+125	$^\circ\text{C}$
V <sub>iso</sub>	Isolation voltage	60Hz, Sinusoidal, 1 minute, All connected pins to heat-sink plate	2500	V <sub>rms</sub>

**Note 2** : T<sub>f</sub> measurement point



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**THERMAL RESISTANCE**

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
R <sub>th(j-f)Q</sub>	Junction to case thermal resistance (Note 3)	Inverter IGBT part (per 1/6 module)	—	—	4.5	°C/W
R <sub>th(j-f)F</sub>		Inverter FWD part (per 1/6 module)	—	—	6.5	°C/W

**Note 3:** Grease with good thermal conductivity should be applied evenly with about +100μm~+200μm on the contacting surface of DIP-IPM and heat-sink.

**ELECTRICAL CHARACTERISTICS** (T<sub>j</sub> = 25°C, unless otherwise noted)

**INVERTER PART**

Symbol	Parameter	Condition	Limits			Unit	
			Min.	Typ.	Max.		
V <sub>CE(sat)</sub>	Collector-emitter saturation voltage	V <sub>D</sub> = V <sub>DB</sub> = 15V I <sub>C</sub> = 15A, T <sub>j</sub> = 25°C	—	1.45	1.95	V	
V <sub>EC</sub>	FWD forward voltage	V <sub>IN</sub> = 5V I <sub>C</sub> = 15A, T <sub>j</sub> = 125°C	—	1.55	2.05	V	
t <sub>on</sub>	Switching times	T <sub>j</sub> = 25°C, -I <sub>C</sub> = 15A, V <sub>IN</sub> = 0V	0.60	1.20	1.80	μs	
t <sub>tr</sub>		V <sub>CC</sub> = 300V, V <sub>D</sub> = V <sub>DB</sub> = 15V	—	0.30	—	μs	
t <sub>c(on)</sub>		I <sub>C</sub> = 15A, T <sub>j</sub> = 125°C, V <sub>IN</sub> = 0 ↔ 5V	—	0.40	0.60	μs	
t <sub>off</sub>		Inductive load (upper-lower arm)	—	1.50	2.10	μs	
t <sub>c(off)</sub>				—	0.50	0.80	μs
I <sub>CES</sub>		Collector-emitter cut-off current	V <sub>CE</sub> = V <sub>CES</sub> T <sub>j</sub> = 25°C	—	—	1	mA
		T <sub>j</sub> = 125°C	—	—	10		

**CONTROL (PROTECTION) PART**

Symbol	Parameter	Condition	Limits			Unit	
			Min.	Typ.	Max.		
I <sub>D</sub>	Circuit current	V <sub>D</sub> = V <sub>DB</sub> = 15V V <sub>IN</sub> = 5V	Total of V <sub>P1</sub> -V <sub>NC</sub> , V <sub>N1</sub> -V <sub>NC</sub>	—	—	5.00	mA
			V <sub>UFB</sub> -V <sub>UFS</sub> , V <sub>VFB</sub> -V <sub>VFS</sub> , V <sub>WFB</sub> -V <sub>WFS</sub>	—	—	0.40	
		V <sub>D</sub> = V <sub>DB</sub> = 15V V <sub>IN</sub> = 0V	Total of V <sub>P1</sub> -V <sub>NC</sub> , V <sub>N1</sub> -V <sub>NC</sub>	—	—	7.00	
			V <sub>UFB</sub> -V <sub>UFS</sub> , V <sub>VFB</sub> -V <sub>VFS</sub> , V <sub>WFB</sub> -V <sub>WFS</sub>	—	—	0.55	
V <sub>FOH</sub>	Fault output voltage	V <sub>SC</sub> = 0V, F <sub>O</sub> circuit pull-up to 5V with 10kΩ	4.9	—	—	V	
V <sub>FOL</sub>		V <sub>SC</sub> = 1V, I <sub>FO</sub> = 1mA	—	—	0.95	V	
V <sub>SC(ref)</sub>	Short circuit trip level	T <sub>f</sub> = -20~100°C, V <sub>D</sub> = 15V (Note 4)	0.45	—	0.52	V	
I <sub>IN</sub>	Input current	V <sub>IN</sub> = 5V	1.0	1.5	2.0	mA	
UV <sub>DBt</sub>	Control supply under-voltage protection	T <sub>j</sub> ≤ 125°C	Trip level	10.0	—		12.0
UV <sub>DBr</sub>			Reset level	10.5	—		12.5
UV <sub>Dt</sub>			Trip level	10.3	—		12.5
UV <sub>Dr</sub>			Reset level	10.8	—		13.0
t <sub>FO</sub>	Fault output pulse width	C <sub>FO</sub> = 22nF (Note 5)	1.0	1.8	—	ms	
V <sub>th(on)</sub>	ON threshold voltage	Applied between UP, VP, WP-V <sub>NC</sub> , UN, VN, WN-V <sub>NC</sub>	2.1	2.3	2.6	V	
V <sub>th(off)</sub>	OFF threshold voltage		0.8	1.4	2.1	V	

**Note 4:** Short circuit protection is functioning only for the lower-arms. Please select the external shunt resistance such that the SC trip-level is less than 2.0 times of the current rating.

**5:** Fault signal is asserted corresponding to a short circuit or lower side control supply under-voltage failure. The fault output pulse width t<sub>FO</sub> depends on the capacitance value of C<sub>FO</sub> according to the following approximate equation : C<sub>FO</sub> = 12.2 × 10<sup>-6</sup> × t<sub>FO</sub> [F].

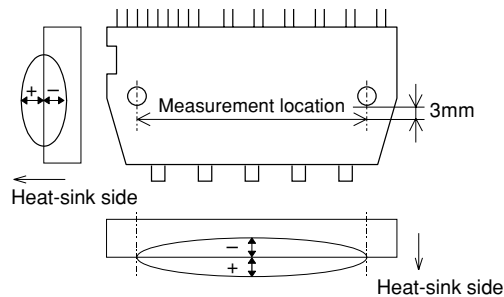
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## MECHANICAL CHARACTERISTICS AND RATINGS

Parameter	Condition		Limits			Unit
			Min.	Typ.	Max.	
Mounting torque	Mounting screw : M3	Recommended : 0.78 N·m	0.59	—	0.98	N·m
Weight			—	20	—	g
Heat-sink flatness	(Note 6)		-50	—	100	μm

**Note 6:** Measurement point of heat-sink flatness



## RECOMMENDED OPERATION CONDITIONS

Symbol	Parameter	Condition	Recommended value			Unit	
			Min.	Typ.	Max.		
V <sub>CC</sub>	Supply voltage	Applied between P-N	0	300	400	V	
V <sub>D</sub>	Control supply voltage	Applied between VP1-V <sub>NC</sub> , VN1-V <sub>NC</sub>	13.5	15.0	16.5	V	
V <sub>DB</sub>	Control supply voltage	Applied between VUFB-VUFS, VVFB-VVFS, VWFB-VWFS	13.0	15.0	18.5	V	
ΔV <sub>D</sub> , ΔV <sub>DB</sub>	Control supply variation		-1	—	1	V/μs	
t <sub>dead</sub>	Arm shoot-through blocking time	For each input signal, T <sub>f</sub> ≤ 100°C	2.0	—	—	μs	
f <sub>PWM</sub>	PWM input frequency	T <sub>f</sub> ≤ 100°C, T <sub>j</sub> ≤ 125°C	—	—	20	kHz	
I <sub>O</sub>	Allowable r.m.s. current	V <sub>CC</sub> = 300V, V <sub>D</sub> = V <sub>DB</sub> = 15V, P.F = 0.8, sinusoidal output T <sub>f</sub> ≤ 100°C, T <sub>j</sub> ≤ 125°C (Note 7)	f <sub>PWM</sub> = 5kHz	—	—	7.5	Arms
			f <sub>PWM</sub> = 15kHz	—	—	4.8	
P <sub>WIN(on)</sub>	Allowable minimum input pulse width	(Note 8)	0.3	—	—	μs	
P <sub>WIN(off)</sub>		Below rated current	0.5	—	—		
		Between rated current and 1.7 times of rated current	2.0	—	—		
	N-line wiring inductance less than 10nH (Note 9)	Between 1.7 times and 2.0 times of rated current	2.6	—	—		
V <sub>NC</sub>	V <sub>NC</sub> variation	Between V <sub>NC</sub> -N (including surge)	-5.0	—	5.0	V	

**Note 7:** The allowable r.m.s. current value depends on the actual application conditions.

**8:** The input pulse width less than P<sub>WIN(on)</sub> might make no response.

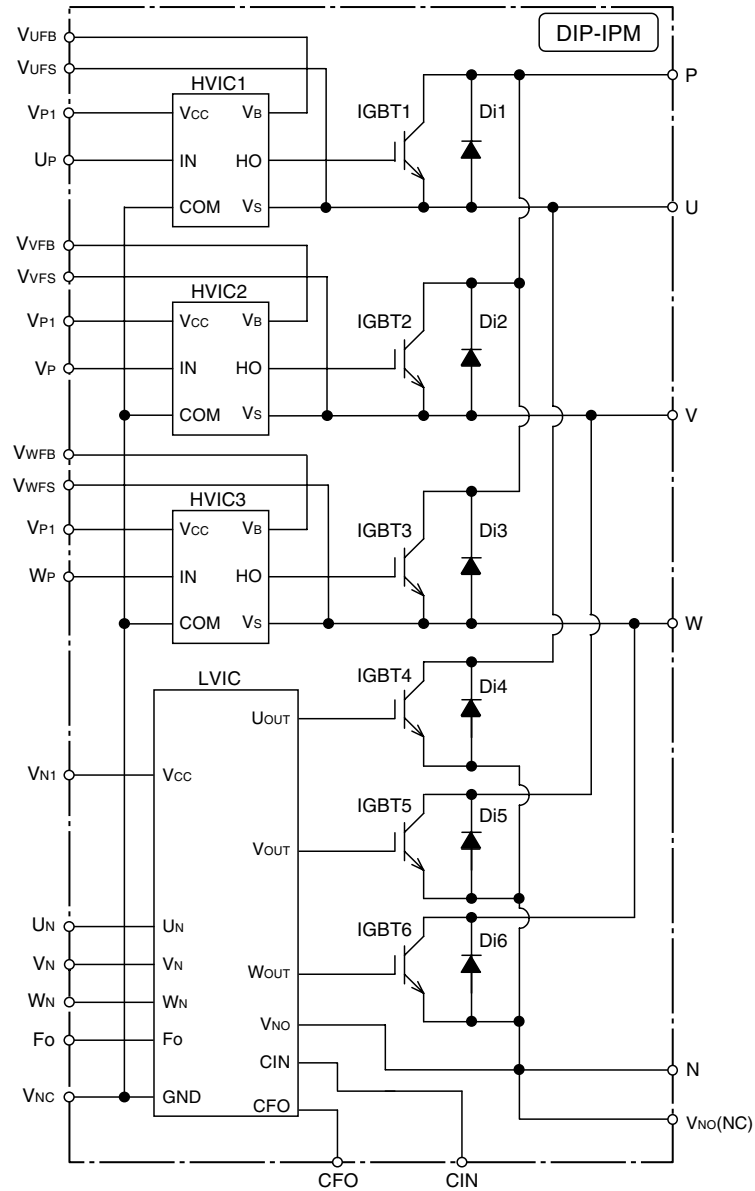
**9:** IPM might not work properly or make response for the input signal with OFF pulse width less than P<sub>WIN(off)</sub>.

Please refer to Fig.7.

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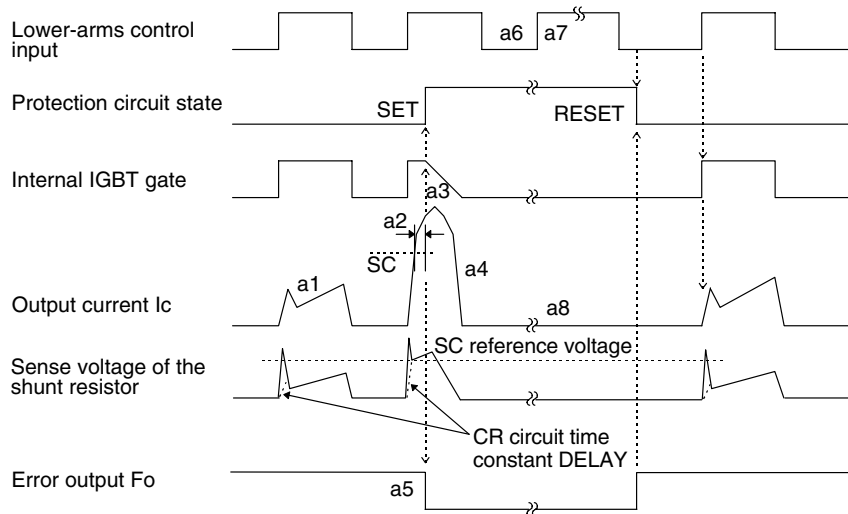
Fig. 4 THE DIP-IPM INTERNAL CIRCUIT



**Fig. 5 TIMING CHART OF THE DIP-IPM PROTECTIVE FUNCTIONS**

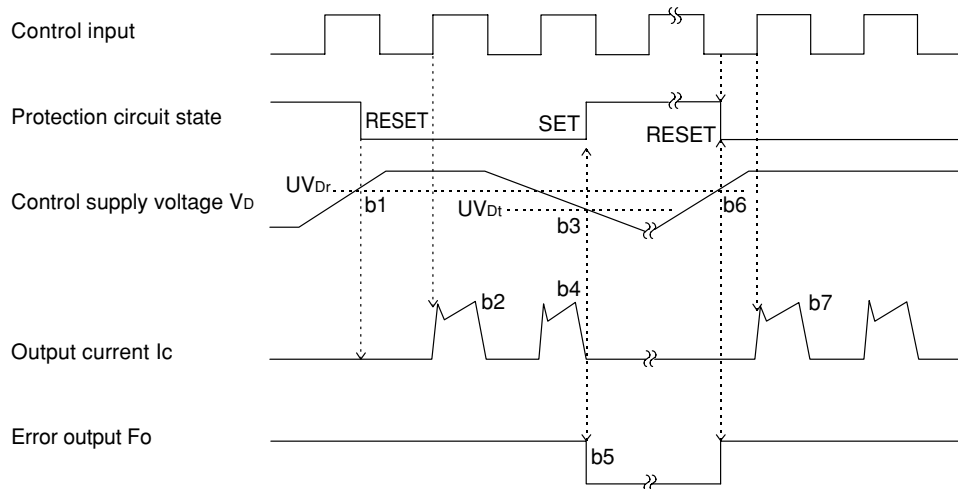
**[A] Short-Circuit Protection (Lower-arms only with the external shunt resistor and CR filter)**

- a1. Normal operation : IGBT ON and carrying current.
- a2. Short circuit current detection (SC trigger).
- a3. IGBT gate hard interruption.
- a4. IGBT turns OFF.
- a5. FO timer operation starts : The pulse width of the Fo signal is set by the external capacitor C<sub>FO</sub>.
- a6. Input "L" : IGBT OFF.
- a7. Input "H" : IGBT ON.
- a8. IGBT OFF in spite of input "H".



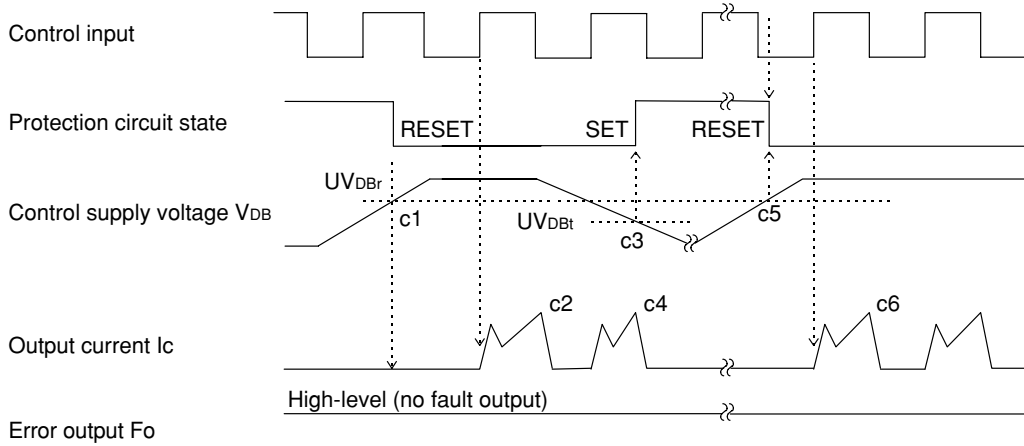
**[B] Under-Voltage Protection (Lower-arm, UVd)**

- b1. Control supply voltage rises : After the voltage level reaches UV<sub>Dr</sub>, the circuits start to operate when next input is applied.
- b2. Normal operation : IGBT ON and carrying current.
- b3. Under voltage trip (UV<sub>Dt</sub>).
- b4. IGBT OFF in spite of control input condition.
- b5. FO operation starts.
- b6. Under voltage reset (UV<sub>Dr</sub>).
- b7. Normal operation : IGBT ON and carrying current.

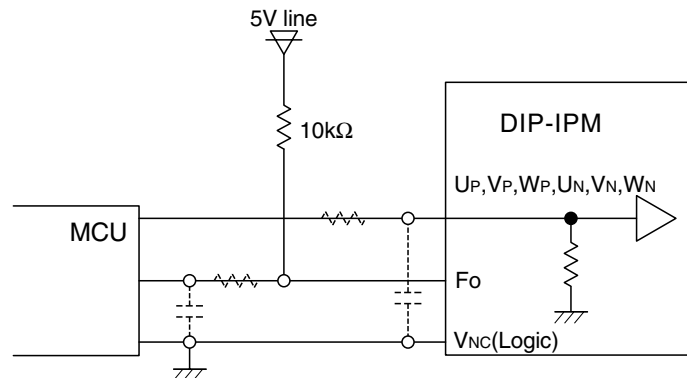


**[C] Under-Voltage Protection (Upper-arm, UVDB)**

- c1. Control supply voltage rises : After the voltage reaches UVDBr, the circuits start to operate when next input is applied.
- c2. Normal operation : IGBT ON and carrying current.
- c3. Under voltage trip (UVDBt).
- c4. IGBT OFF in spite of control input condition, but there is no Fo signal output.
- c5. Under voltage reset (UVDBr).
- c6. Normal operation : IGBT ON and carrying current.



**Fig. 6 RECOMMENDED CPU I/O INTERFACE CIRCUIT**



**Note :** The setting of RC coupling at each input (parts shown dotted) depends on the PWM control scheme and the wiring impedance of the printed circuit board.  
The DIP-IPM input section integrates a 2.5kΩ (min) pull-down resistor. Therefore, when using an external filtering resistor, pay attention to the turn-on threshold voltage.

**Fig. 7 WIRING CONNECTION OF SHUNT RESISTOR**

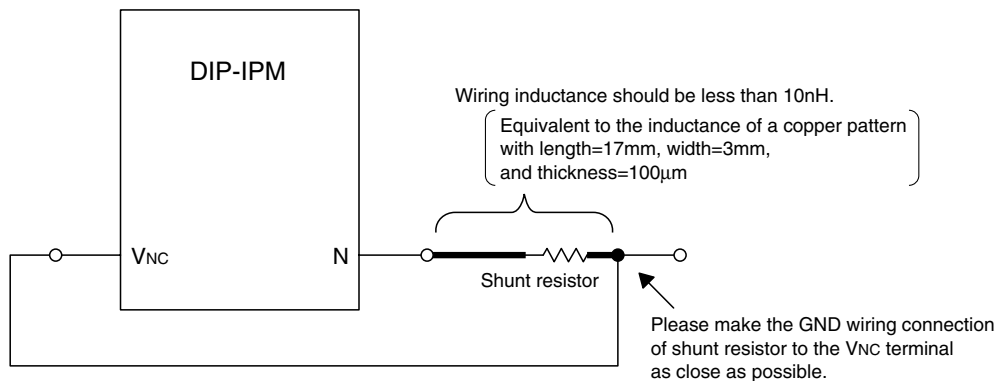
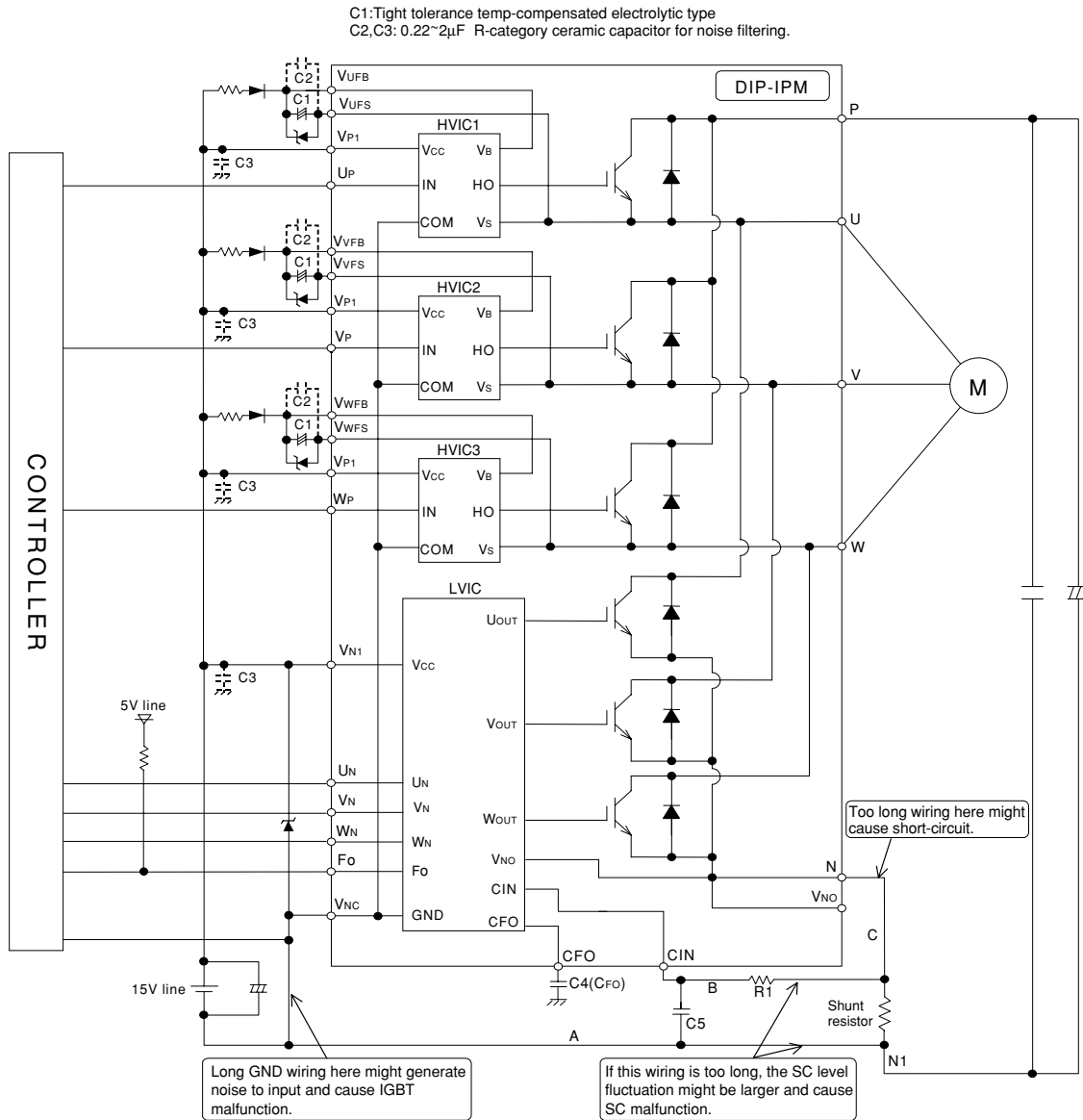




Fig. 8 TYPICAL DIP-IPM APPLICATION CIRCUIT EXAMPLE



**Note 1:** To prevent the input signals oscillation, the wiring of each input should be as short as possible. (Less than 2cm)

- 2: By virtue of integrating an application specific type HVIC inside the module, direct coupling to MCU terminals without any opto-coupler or transformer isolation is possible.
- 3: Fo output is open drain type. This signal line should be pulled up to the positive side of the 5V power supply with approximately 10kΩ resistor.
- 4: Fo output pulse width is determined by the external capacitor between CFO and Vnc terminals (CFO). (Example : CFO = 22 nF → tFO = 1.8 ms (typ.))
- 5: The logic of input signal is high-active. The DIP-IPM input signal section integrates a 2.5kΩ (min) pull-down resistor. Therefore, when using external filtering resistor, care must be taken to satisfy the turn-on threshold voltage requirement.
- 6: To prevent malfunction of protection, the wiring of A, B, C should be as short as possible.
- 7: Please set the C5R1 time constant in the range 1.5~2μs.
- 8: Each capacitor should be located as nearby the pins of the DIP-IPM as possible.
- 9: To prevent surge destruction, the wiring between the smoothing capacitor and the P, N1 pins should be as short as possible. Approximately a 0.1~0.22μF snubber capacitor between the P-N1 pins is recommended.
- 10: Please leave VNO open. (no connect)
- 11: To prevent ICs from surge destruction, it is recommended to insert a Zener diode (24V, 1W) nearby each pair of supply terminals.