NTE1254
Integrated Circuit
Phase–Lock Loop (PLL) Frequency
Synthesizer for CB

Features:

- Programmable Divider – Divided by 3 to 255
- 10–Bit Divider
- Phase Detector
- Reference Oscillation Circuit
- On–Chip Filter Amplifier
- Code Converter
- Only two or three crystals required for CB radio AM frequency selection
- Unlocked signals are detected at instant stop "IS" terminal
- Two type program mode can be selected to change input mode level
    M: Low level .   Binary code input enables, divided by 3 to 255
    M: High level .   BCD code enables that the data at P_1 to P_6 port is offset 90 by code converter
- Internal active filter amplifier has a long holding time due to very high input impedance characteristics of the CMOS–this is to obtain very good spurious response.
- Output signal of the "I" can be used to stop the spurious radiation when the channel selector makes misprogramming such as rotary switch's lose contact.
- High speed and low power consumption due to CMOS
- Single power supply and fully TTL compatible: V_{DD} = 5 ± 0.5 Volts
- Operating Temperature: T_A = –30° to 65°C
- Pull down resistors installed in program and mode switch inputs

Absolute Maximum Ratings:

Supply Voltage . . . . –0.3 to +6.0V
Input Voltage . . . . –0.3 to +6.0V
Operating Temperature Range, T_{opr} . . . . –35° to +75°C
Storage Temperature Range, T_{stg} . . . . –55° to +125°C

Electrical Characteristics: $(T_A = -35°$ to $+75°C$ unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Supply	V_{DD}		4.5	5.0	5.5	V
Total Current	I_{DD}	f = 0	–	–	10	mA
High Level Input Voltage	V_{IH}	All Inputs	$0.8V_{DD}$	–	V_{DD}	V
Low Level Input Voltage	V_{IL}	All Inputs	–0.3	–	$0.2V_{DD}$	V
High Level Output Voltage	V_{OH}	All Outputs Except D_2, $I_O = -0.3mA$, $V_{DD} = 4.5V$	$0.85V_{DD}$	–	V_{DD}	V
		$I_O = -0.15mA$, $V_{DD} = 4.5V$	$0.85V_{DD}$	–	V_{DD}	V
Low Level Output Voltage	V_{OL}	All Inputs, $I_O = 0.5mA$, $V_{DD} = 4.5V$	–0.3	–	$0.15V_{DD}$	V
Leakage Current	I_L	EO (Floating), Al $T_A = +25°C$	–	1.0	–	nA
Input Capacitance	C_i	PI, FD, FP, X_1, $V_i = 0$	–	–	10	pF
Maximum Frequency Response	$f_d$max	$X_1 - X_2$, Divider	11	–	–	MHz
	$f_p$max	Programmable Divider	–	2	–	MHz

Pin Connection Diagram

Program Input P1	1	24 Inhibit Output
Program Input P2	2	23 V_{SS}
Program Input P3	3	22 Instant Stop
Program Input P4	4	21 Phase Error Output
Program Input P5	5	20 Filter Amp Input
Program Input P6	6	19 Filter Amp Output
Program Input P7	7	18 Detector Input
Program Input P8	8	17 Divider Output
1/2 Output Reference	9	16 Detector Input
X'tal Input	10	15 Divider Output
X'tal Input	11	14 Input Mode Switch
V_{DD}	12	13 Divider Input

24 ... 13

1 ... 12

1.300 (33.02) Max

.520 (13.2)

.225 (5.73) Max

.100 (2.54)

1.100 (27.94)

.126 (3.22) Min

.600 (15.24)