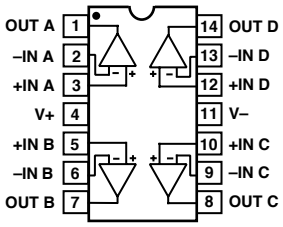
Quad Matched 741-Type Operational Amplifiers

OP11

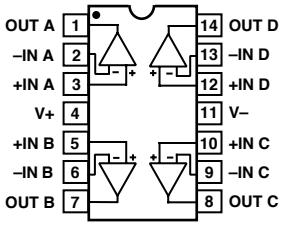
FEATURES
Guaranteed V_{OS}: 500 μV Max
Guaranteed Matched CMRR: 94 dB Min
Guaranteed Matched V_{OS}: 750 μV Max
LM148/LM348 Direct Replacement
Low Noise
Silicon-Nitride Passivation
Internal Frequency Compensation
Low Crossover Distortion
Continuous Short-Circuit Protection
Low Input Bias Current

PIN CONFIGURATIONS

14-Lead Epoxy DIP
(P Suffix)



14-Lead Hermetic DIP
(Y Suffix)



GENERAL DESCRIPTION

The OP11 provides four matched 741-type operational amplifiers in a single 14-lead DIP package. The OP11 is pin compatible with the LM148, LM348, RM4156, RM4158, and HA4741 amplifiers. The amplifier is matched for common-mode rejection ratio and offset voltage which is very important in designing instrumentation amplifiers. In addition, the amplifier is designed to have equal positive-going and negative-going slew rates. This is an important consideration for good audio system performance.

The OP11 is ideal for use in designs requiring minimum space and cost while maintaining performance.

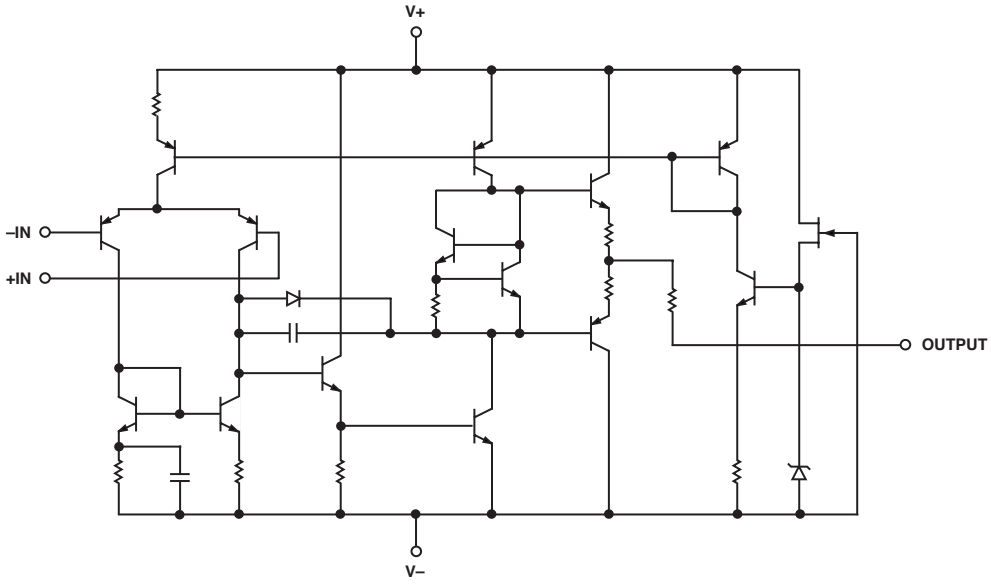


Figure 1. Simplified Schematic

REV. A

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OP11–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_S = ±15 V, T_A = 25°C, unless otherwise noted)

Parameter	Symbol	Conditions	OP11A/OP11E Min	OP11A/OP11E Typ	OP11A/OP11E Max	OP11F Min	OP11F Typ	OP11F Max	OP11G Min	OP11G Typ	OP11G Max	Unit
Input Offset Voltage	V_{OS}	R_S = 10 kΩ		0.3	0.5		0.6	2.5		1.2	5.0	mV
Input Offset Current	I_{OS}			5.5	20		25	50		75	200	nA
Input Bias Current	I_B			180	300		300	500		300	500	nA
Input Resistance Differential Mode[1]	R_{IN}		0.17	0.29		0.1	0.17		0.1	0.17		MΩ
Input Voltage Range	IVR		±12	±13		±12	±13		±12	±13		V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±12 V, R_S = 10 kΩ	100	120		100	120		70	100		dB
Power Supply Rejection Ratio	PSRR	V_S = ±5 V to ±15 V, R_S ≤ 10 kΩ		4	32		4	32		10	100	µV/V
Output Voltage Swing	V_O	R_L = 2 kΩ	±11	±13		±11	±13		±11	±13		V
Large-Signal Voltage Gain	A_{VO}	R_L ≤ 2 kΩ, V_O = ±10 V	100	650		100	650		50	500		V/mV
Power Consumption[2]	P_d	V_O = 0 V		105	180		123	180		210	340	mW
Input Noise Voltage	e_n p-p	0.1 Hz to 10 Hz		0.7			0.7			0.7		µV p-p
Input Noise Voltage Density	e_n	f_O = 10 Hz f_O = 100 Hz f_O = 1 MHz		18 14 12			18 14 12			18 14 12		nV/√Hz nV/√Hz nV/√Hz
Input Noise Current	I_n p-p	0.1 Hz to 10 Hz		17			17			17		pA p-p
Input Noise Current Density	I_n	f_O = 10 Hz f_O = 100 Hz f_O = 1 MHz		1.8 1.5 1.2			1.8 1.5 1.2			1.8 1.5 1.2		pA/√Hz pA/√Hz pA/√Hz
Channel Separation	CS		100	130		100	130			130		dB
Slew Rate[2]	SR		0.7	1.0		0.7	1.0		0.7	1.0		V/µs
Large Signal Bandwidth[3]		V_O = 20 V p-p	11	16		11	16		11	16		kHz
Closed-Loop Bandwidth[4]	BW	A_{VCL} = 1	2.4	3.0		2.4	3.0		2.4	3.0		MHz
Rise Time[3]	t_f	A_V = 1, V_{IN} = 50 mV		110	145		110	145		110	145	ns
Overshoot[3]	OS			15	25		15	25		15	25	%

NOTES
[1]Guaranteed by input bias current.
[2]Total dissipation for all four amplifiers in package.
[3]Sample tested.
[4]Guaranteed by rise time.

Specifications subject to change without notice

ELECTRICAL CHARACTERISTICS (@ V_S = ±15 V, −55°C ≤ T_A ≤ +125°C for OP11A, 0°C ≤ T_A ≤ 70°C for OP11E, unless otherwise noted)

Parameter	Symbol	Conditions	OP11A Min	OP11A Typ	OP11A Max	OP11E Min	OP11E Typ	OP11E Max	Unit
Input Offset Voltage	V_{OS}	R_S ≤ 10 kΩ		0.4	1.0		0.4	0.8	mV
Average Input Offset Voltage Drift[1]	TCV_{OS}	R_S ≤ 10 kΩ		2.0	10		2.0	10	µV/°C
Input Offset Current	I_{OS}			20	40		14	30	nA
Average Input Offset Current Drift[1]	TCI_{OS}			0.1	0.3		0.1	0.3	nA/°C
Input Bias Current	I_B			200	375		200	350	nA
Input Voltage Range	IVR		±12	±13		±12	±13		V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±12 V, R_S ≤ 10 kΩ	100	120		100	120		dB
Power Supply Rejection Ratio	PSRR	V_S = ±5 V to ±15 V, R_S ≤ 10 kΩ		4	32		4	32	µV/V
Large-Signal Voltage Gain	A_{VO}	R_L ≥ 2 kΩ, V_O = ±10 V	50	250		50	250		V/mV
Output Voltage Swing	V_O	R_L ≥ 2 kΩ	±11	±13		±11	±13		V
Power Consumption[2]	P_d	V_O = 0 V		115	200		115	200	mW

NOTES
[1]Guaranteed but not tested.
[2]Total dissipation for all four amplifiers in package.
Specifications subject to change without notice

ELECTRICAL CHARACTERISTICS (@ V_S = ±15 V, −40°C ≤ T_A ≤ +85°C, R_S ≤ 100 Ω, unless otherwise noted)

Parameter	Symbol	Conditions	OP11F Min	OP11F Typ	OP11F Max	OP11G Min	OP11G Typ	OP11G Max	Unit
Input Offset Voltage	V_{OS}	R_S ≤ 10 kΩ		0.8	3.0		1.5	6 .0	mV
Average Input Offset Voltage Drift	TCV_{OS}	R_S ≤ 10 kΩ		4.0	15		4.0		µV/°C
Input Offset Current	I_{OS}			40	60		250	300	nA
Average Input Offset Current Drift[1]	TCI_{OS}			0.3	0.6		0.3	0.6	nA/°C
Input Bias Current	I_B			400	550		400	800	nA
Input Voltage Range	IVR		±12	±13		±12	±13		V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±12 V, R_S ≤ 10 kΩ	100	120		70	100		dB
Power Supply Rejection Ratio	PSRR	V_S = ±5 V to ±15 V, R_S ≤ 10 kΩ		4	32		10	100	µV/V
Large-Signal Voltage Gain	A_{VO}	R_L ≥ 2 kΩ, V_O = ±10 V	50	250		25	100		V/mV
Output Voltage Swing	V_O	R_L ≥ 2 kΩ	±11	±13		±11	±13		V
Power Consumption[2]	P_d	V_O = 0 V		115	200		250	400	mW

NOTES
[1]Guaranteed but not tested.
[2]Total dissipation for all four amplifiers in package.
Specifications subject to change without notice

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage (V_S) . . . . . ±22 V
Input Voltage* . . . . . Supply Voltage
Differential Input Voltage . . . . . ±30 V
Output Short-Circuit Duration . . . . . Continuous (One Amp Only)
Storage Temperature Range
  Y Package . . . . . –65°C to +150°C
  P Package . . . . . –65°C to +125°C
Lead Temperature Range (Soldering, 60 sec) . . . . . 300°C
Operating Temperature Range
  OP11A . . . . . –55°C to +125°C
  OP11E . . . . . 0°C to 70°C
  OP11F, OP11G . . . . . –40°C to +85°C

*Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.

Package Type	θ_{JA}*	θ_{JC}	Unit
14-Lead Plastic DIP (P)	83	39	°C/W
14-Lead Hermetic DIP (Y)	108	15	°C/W

*θ_{JA} is specified for worst-case conditions, i.e., θ_{JA} is specified for device in socket for CERDIP and P-DIP packages.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
OP11AY*	–40°C to +125°C	14-Lead CERDIP	Y-14
OP11EP	–40°C to +125°C	14-Lead Epoxy DIP	P-14
OP11EY*	0°C to 85°C	14-Lead CERDIP	Y-14
OP11FP*	–40°C to 85°C	14-Lead Epoxy DIP	P-14
OP11GP	–40°C to 85°C	14-Lead Epoxy DIP	P-14

*Not for new designs. Obsolete April 2002.

For Military processed devices, please refer to the Standard Microcircuit Drawing (SMD) available at www.dscc.dla.mil/programs/milspec/default.asp

SMD Part Number	ADI Equivalent
5962-89801012A	OP11ARCMDA
5962-8980101CA	OP11AYMDA

MATCHING CHARACTERISTICS (@ V_S = ±15 V, T_A = 25°C, $R_S \leq 100\ \Omega$, unless otherwise noted)

Parameter	Symbol	Conditions	OP11A, OP11E Min	OP11A, OP11E Typ	OP11A, OP11E Max	OP11F Min	OP11F Typ	OP11F Max	Unit
Input Offset Voltage Match	ΔV_{OS}			0.5	0.75		0.6	2.0	mV
Common-Mode Rejection Ratio Match	ΔCMRR	V_{CM} = ±12 V		1	20		1	20	µV/V
		V_{CM} = ±12 V	94	120		94	120		dB

Specifications subject to change without notice

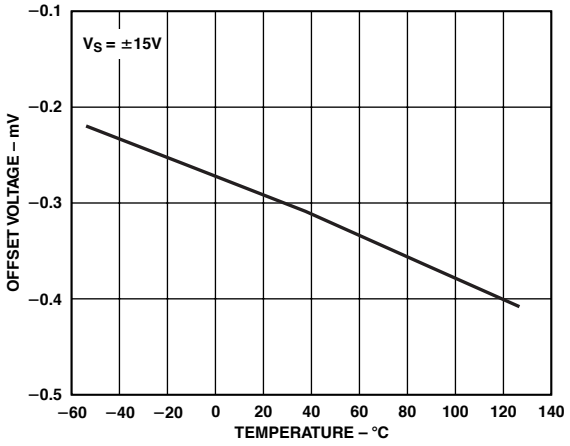
MATCHING CHARACTERISTICS (@ V_S = ±15 V, −55°C ≤ T_A ≤ +125°C for OP11A, 0°C ≤ T_A ≤ 70°C for OP11E, −40°C ≤ T_A ≤ +85°C for OP11F, $R_S \leq 100\ \Omega$, unless otherwise noted)

Parameter	Symbol	Conditions	OP11A, OP11E Min	OP11A, OP11E Typ	OP11A, OP11E Max	OP11F Min	OP11F Typ	OP11F Max	Unit
Input Offset Voltage Match	ΔV_{OS}			0.6	1.0		1.0	2.5	mV
Common-Mode Rejection Ratio Match	ΔCMRR	V_{CM} = ±12 V		3.2	20		3.2	20	µV/V
		V_{CM} = ±12 V	94	110		94	110		dB

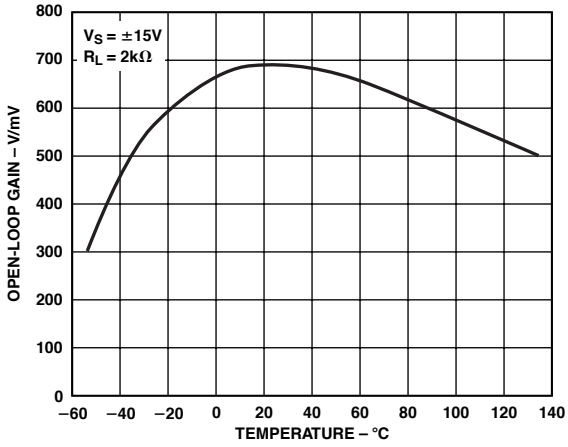
Specifications subject to change without notice

CAUTION

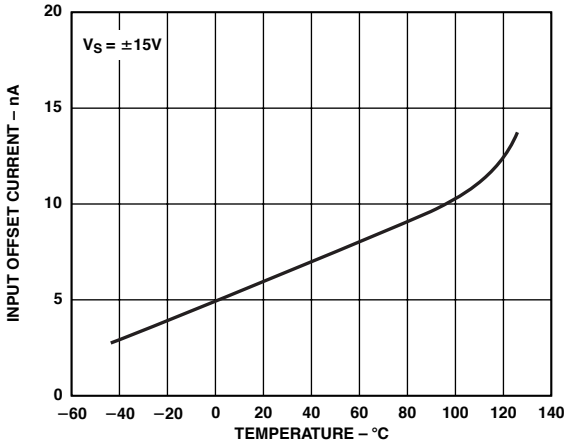
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the OP11 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



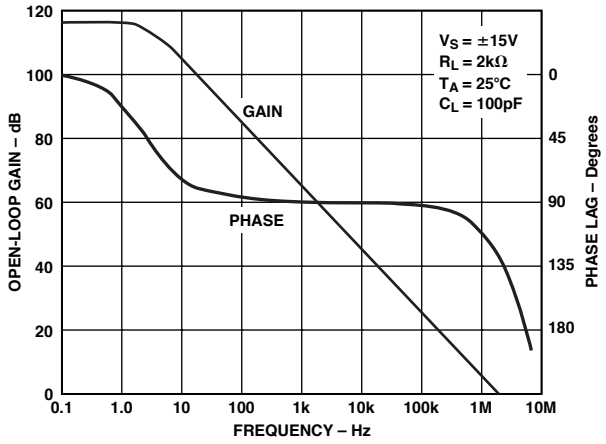
TPC 1. Input Offset Voltage vs. Temperature



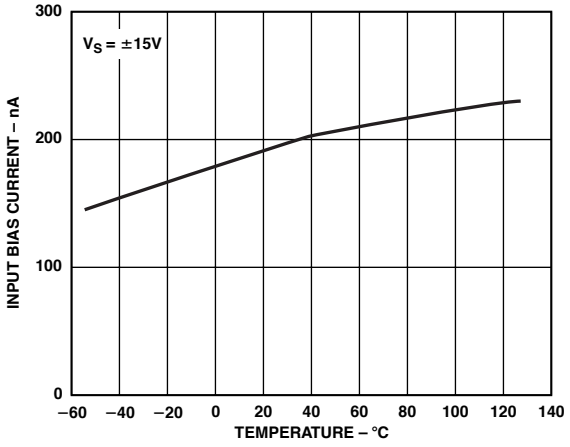
TPC 4. Open-Loop Gain vs. Temperature



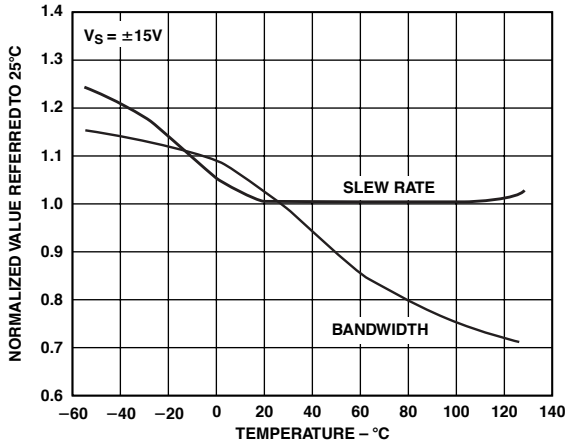
TPC 2. Offset Current vs. Temperature



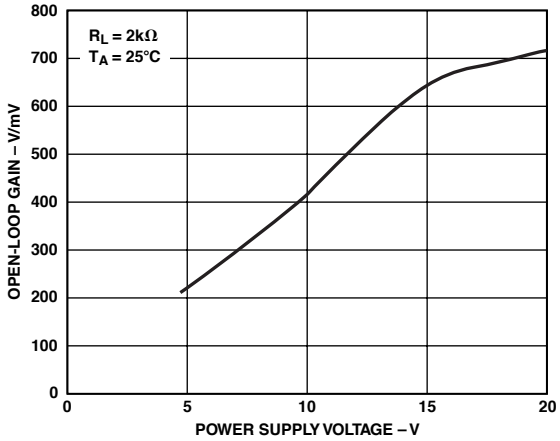
TPC 5. Open-Loop Gain and Phase vs. Frequency



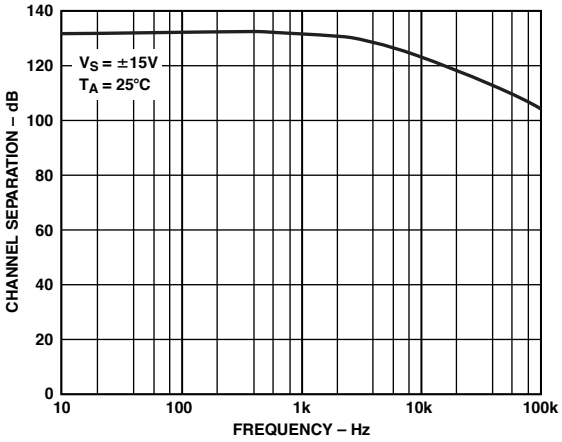
TPC 3. Bias Current vs. Temperature



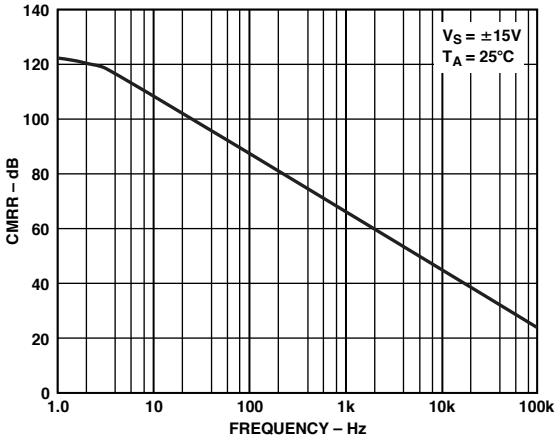
TPC 6. Normalized Slew Rate and Bandwidth vs. Temperature



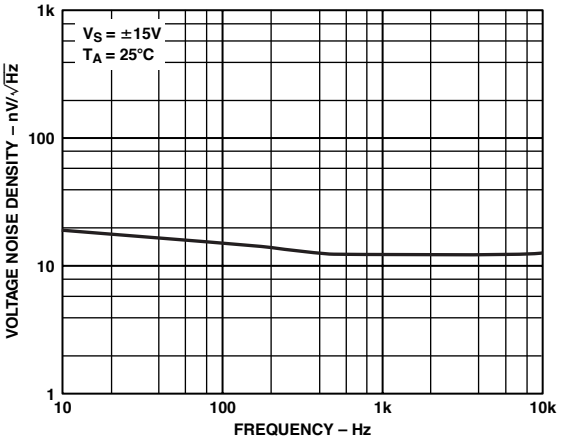
TPC 7. Open-Loop Gain vs. Supply Voltage



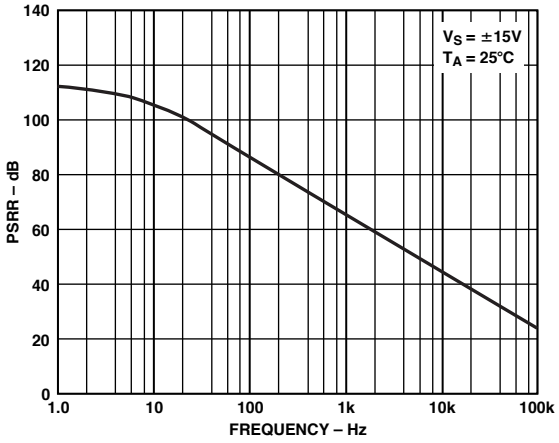
TPC 10. Channel Separation vs. Frequency



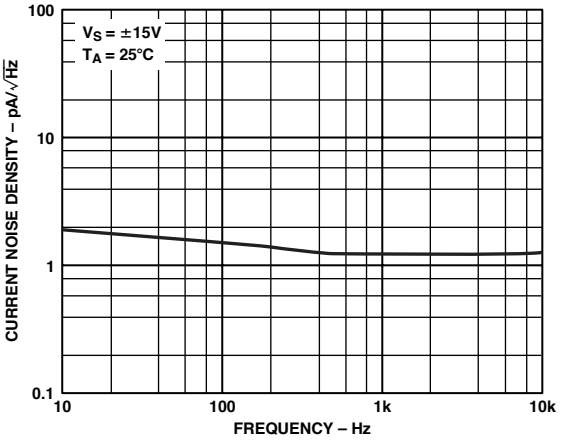
TPC 8. CMRR vs. Frequency



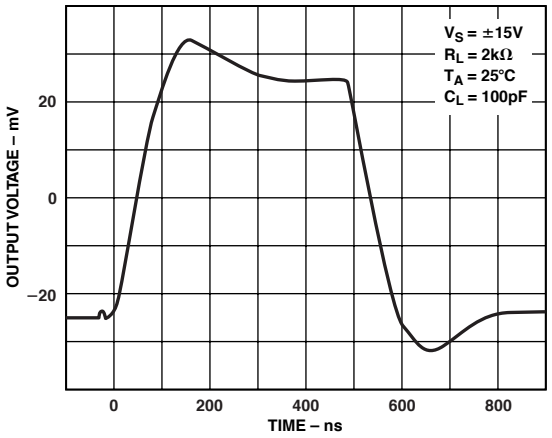
TPC 11. Voltage Noise Density vs. Frequency



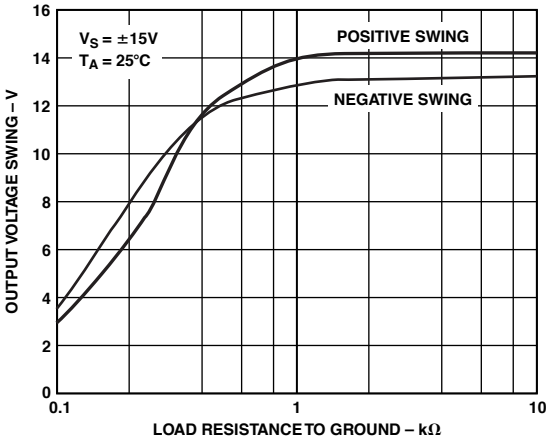
TPC 9. PSRR vs. Frequency



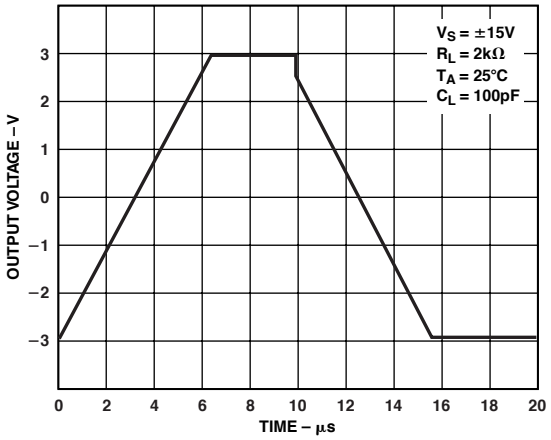
TPC 12. Noise Current Density vs. Frequency



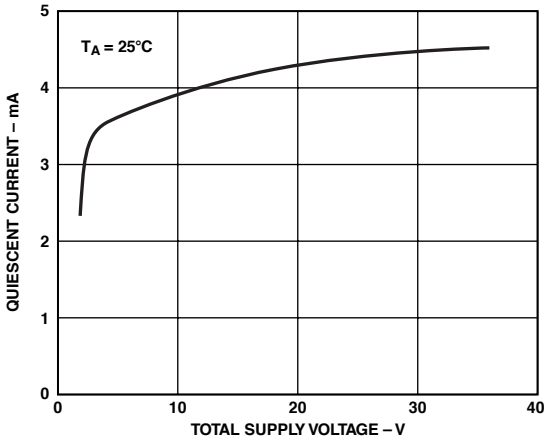
TPC 13. Transient Response



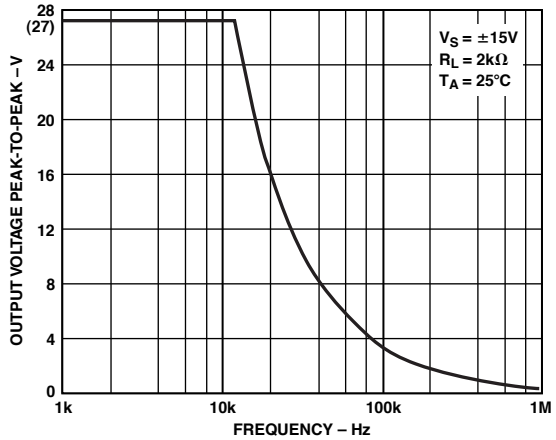
TPC 16. Output Voltage vs. Load Resistance



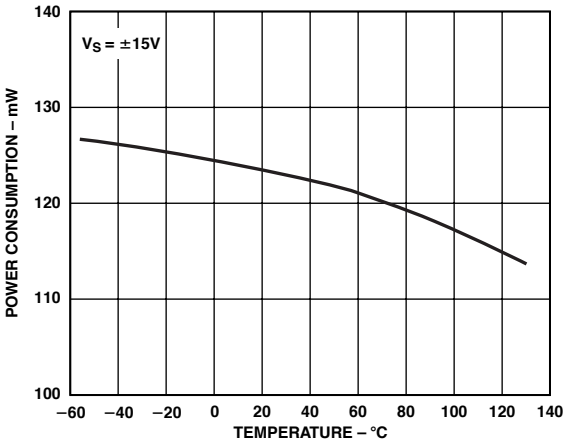
TPC 14. Voltage Follower Pulse Response



TPC 17. Quiescent Current vs. Supply Voltage



TPC 15. Maximum Output Swing vs. Frequency

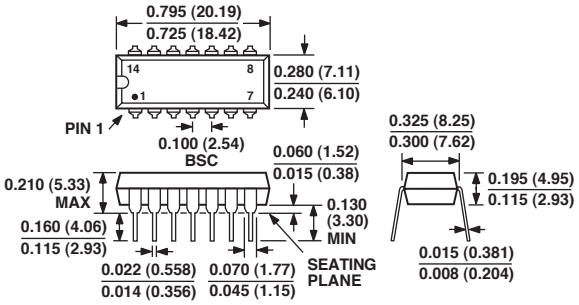


TPC 18. Power Consumption vs. Temperature

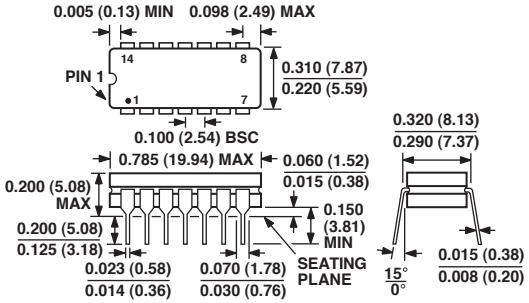
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

14-Lead Epoxy DIP
(P Suffix)



14-Lead Hermetic DIP
(Y Suffix)



Revision History

Location	Page
Data Sheet changed from REV. 0 to REV. A.	
Change OP-09/OP-11 to OP11	Global
Edits to PIN CONNECTIONS	1
Edits to Figure 1	1
Edits to ABSOLUTE MAXIMUM RATINGS	2
Edits to ORDERING GUIDE	2
Edits to SPEC TABLES	2-4
Deletion of DICE CHARACTERISTICS	5
Deletion of WAFER TEST LIMITS Table	5
Deletion of TYPICAL ELECTRICAL CHARACTERISTICS Table	5

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